FIGURE 1A

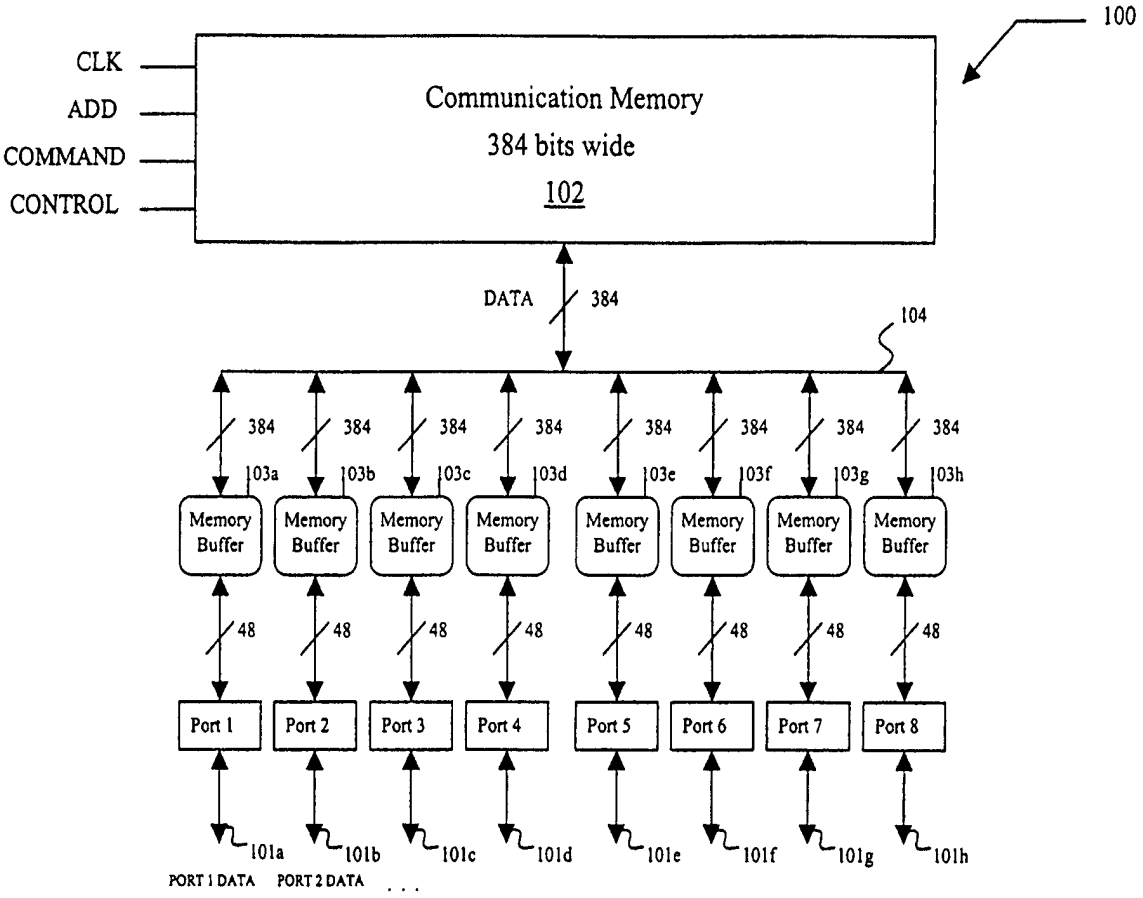
100
CLK
ADD
COMMAND
CONTROL
Communication Memory
384 bits wide
102
DATA
384
104
384
103a
103b
103c
103d
103e
103f
103g
103h
Memory Buffer
48
Port 1
Port 2
Port 3
Port 4
Port 5
Port 6
Port 7
Port 8
101a
101b
101c
101d
101e
101f
101g
101h
PORT 1 DATA
PORT 2 DATA

FIGURE 1B

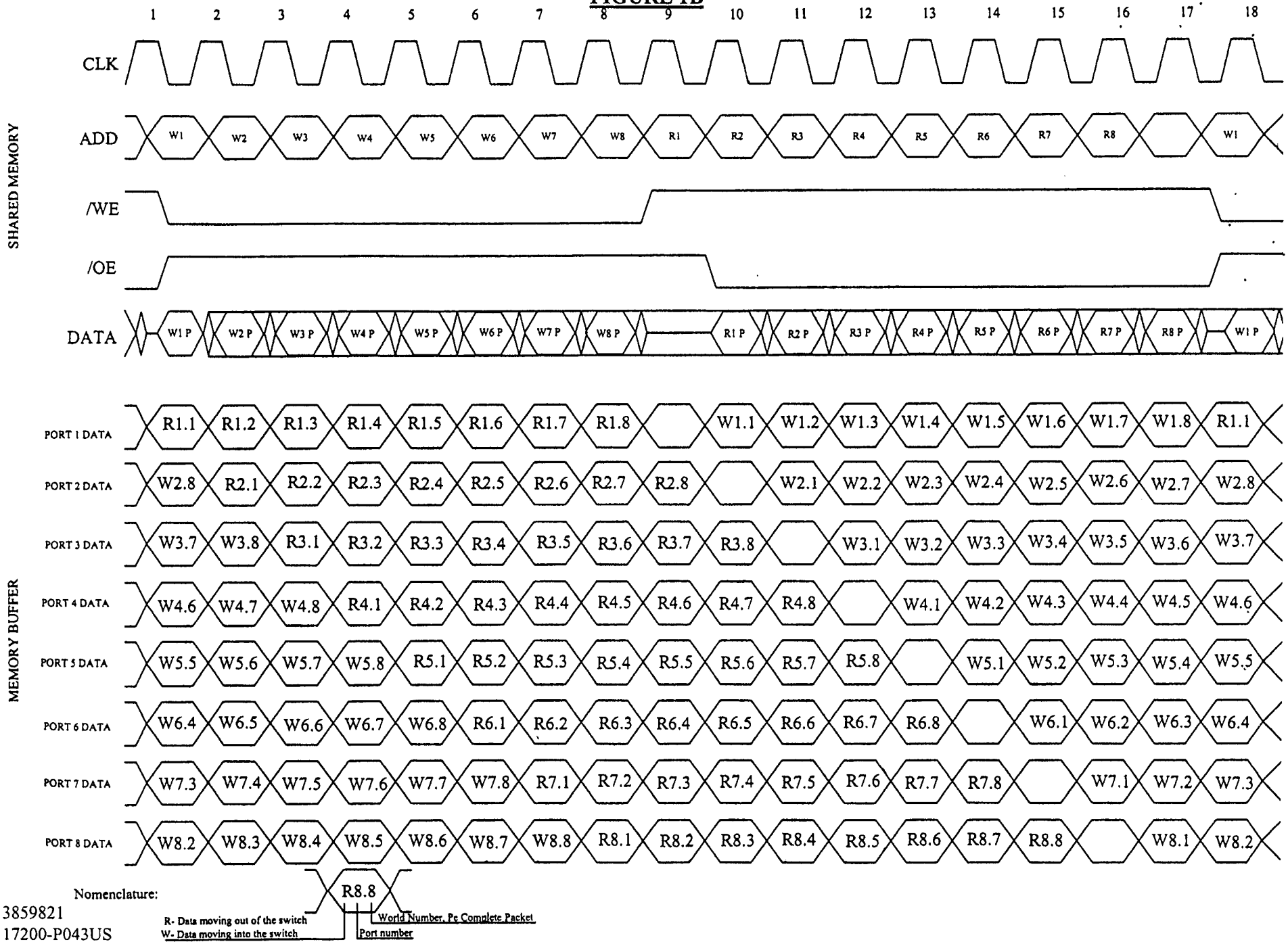

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FIGURE 2A

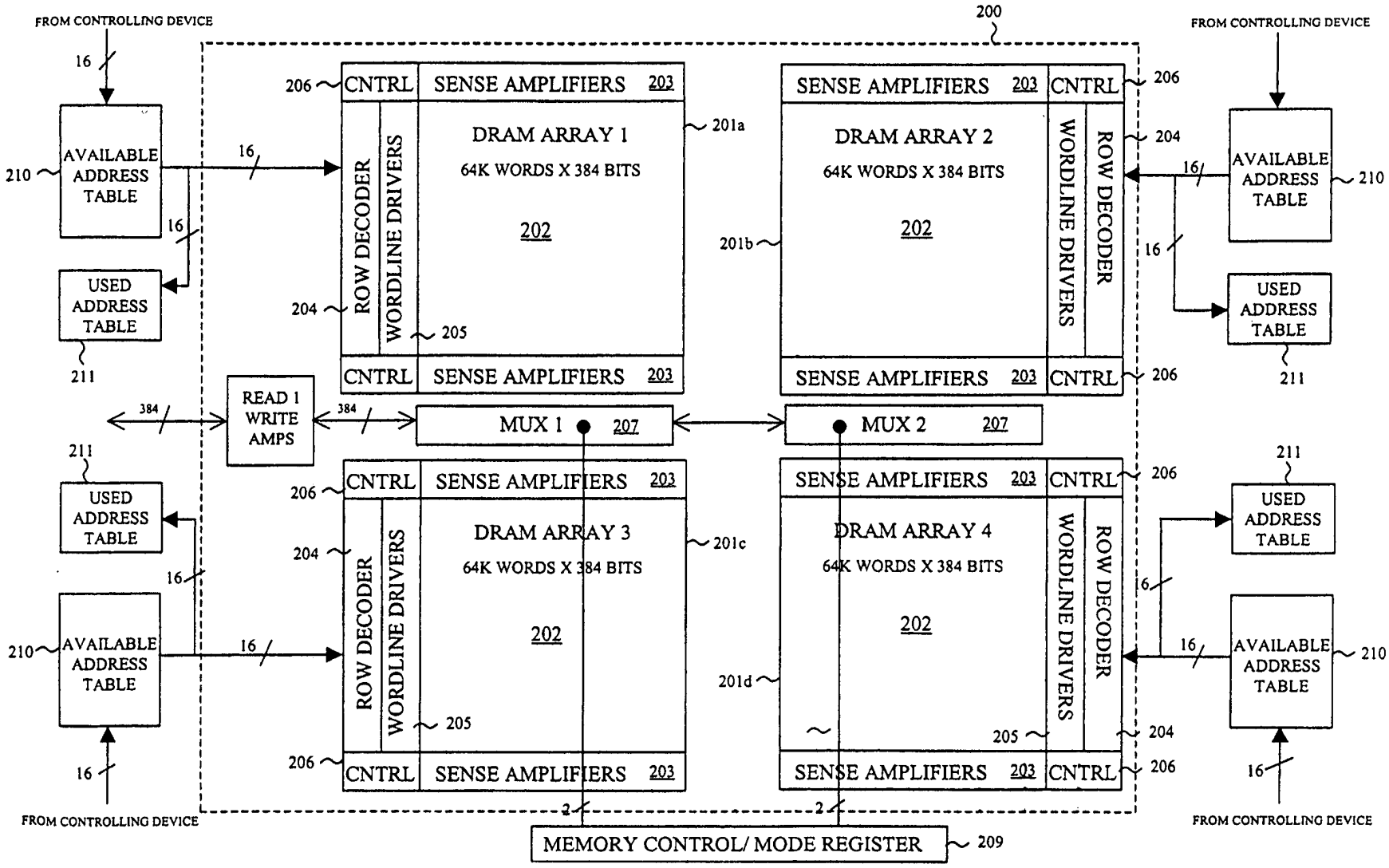
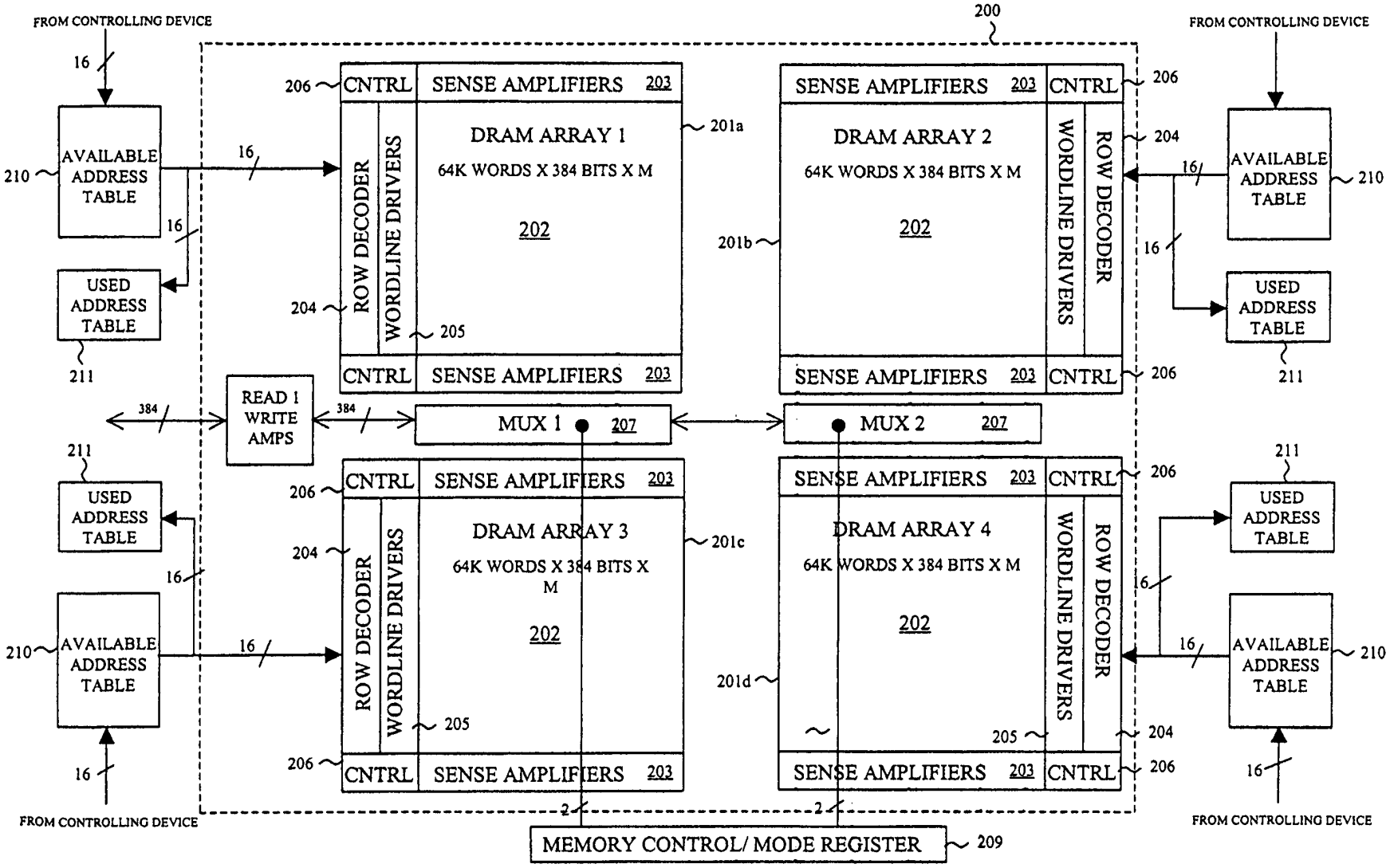
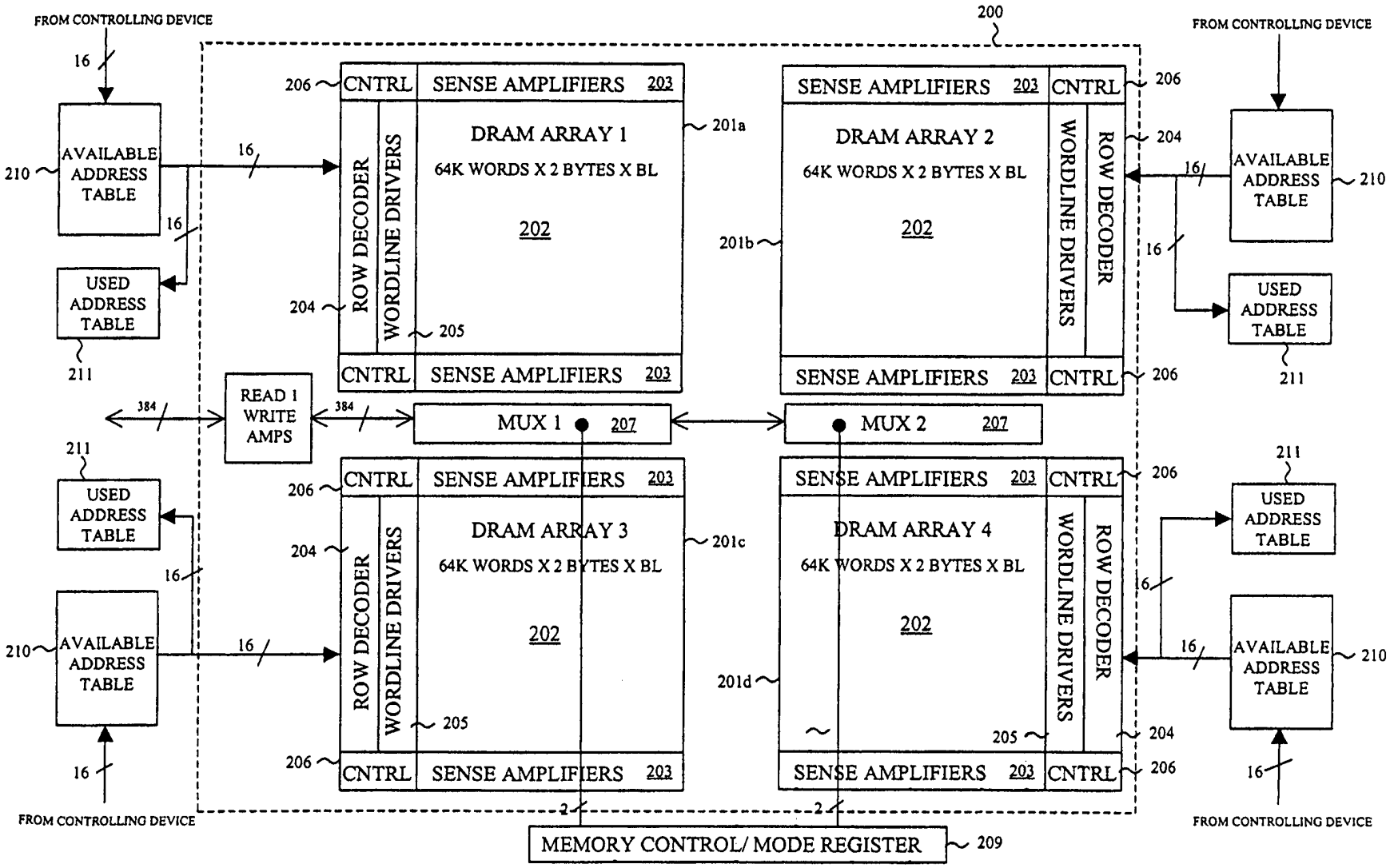

FROM CONTROLLING DEVICE
16
AVAILABLE ADDRESS TABLE
210
USED ADDRESS TABLE
211
200
206
CNTRL
SENSE AMPLIFIERS 203
ROW DECODER
WORDLINE DRIVERS
DRAM ARRAY 1
64K WORDS X 384 BITS
202
201a
204
205
DRAM ARRAY 2
201b
384
READ 1 WRITE AMPS
MUX 1 207
MUX 2 207
DRAM ARRAY 3
201c
DRAM ARRAY 4
201d
2
MEMORY CONTROL/ MODE REGISTER
209

FIGURE 2B



'M' signifies the number of "column decoder groups".

FIGURE 2C



BL = 2, 4, 6, 8, 16 where BL represents burst length.

FIGURE 3A

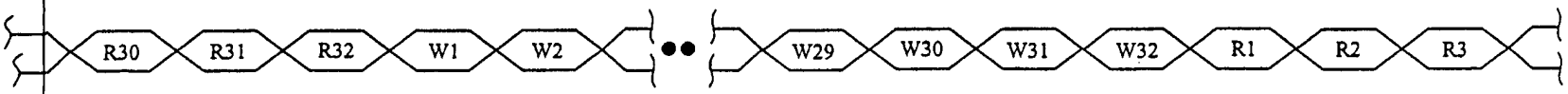


FIGURE 3B

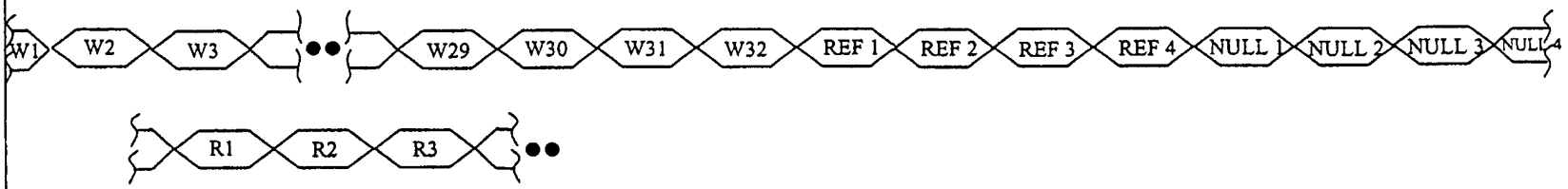


FIGURE 3C

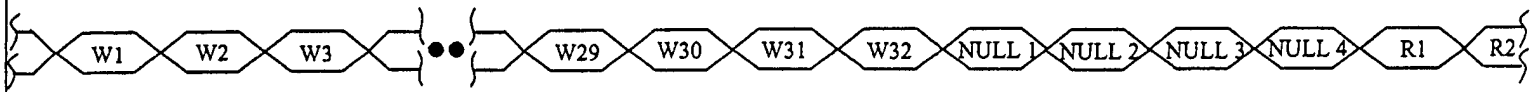


FIGURE 4

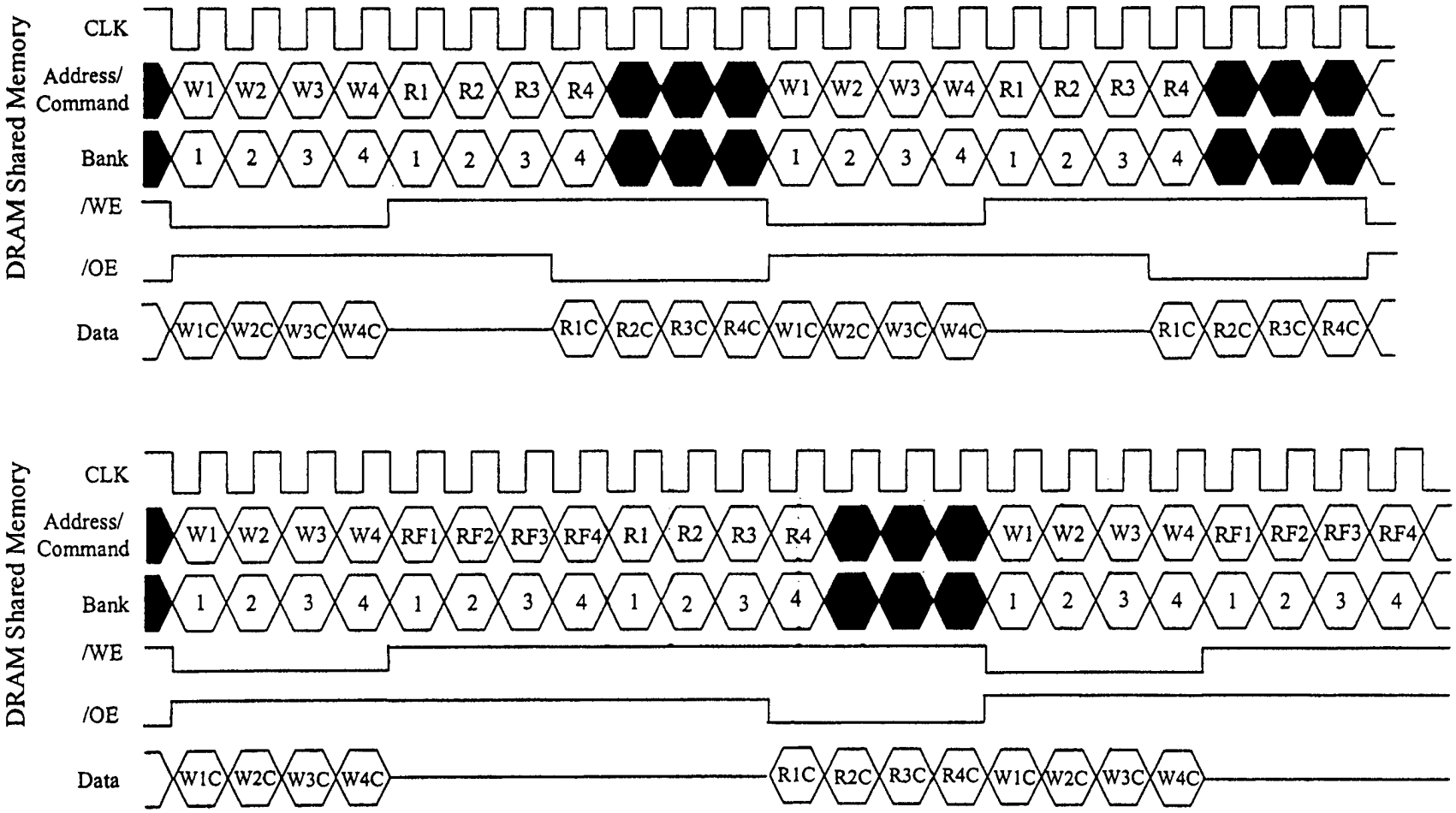

DRAM Shared Memory
CLK
Address/ Command
W1 W2 W3 W4 R1 R2 R3 R4 W1 W2 W3 W4 R1 R2 R3 R4
Bank
1 2 3 4 1 2 3 4 1 2 3 4 1 2 3 4
/WE
/OE
Data
W1C W2C W3C W4C R1C R2C R3C R4C W1C W2C W3C W4C R1C R2C R3C R4C
DRAM Shared Memory
CLK
Address/ Command
W1 W2 W3 W4 RF1 RF2 RF3 RF4 R1 R2 R3 R4 W1 W2 W3 W4 RF1 RF2 RF3 RF4
Bank
1 2 3 4 1 2 3 4 1 2 3 4 1 2 3 4 1 2 3 4
/WE
/OE
Data
W1C W2C W3C W4C R1C R2C R3C R4C W1C W2C W3C W4C

FIGURE 5

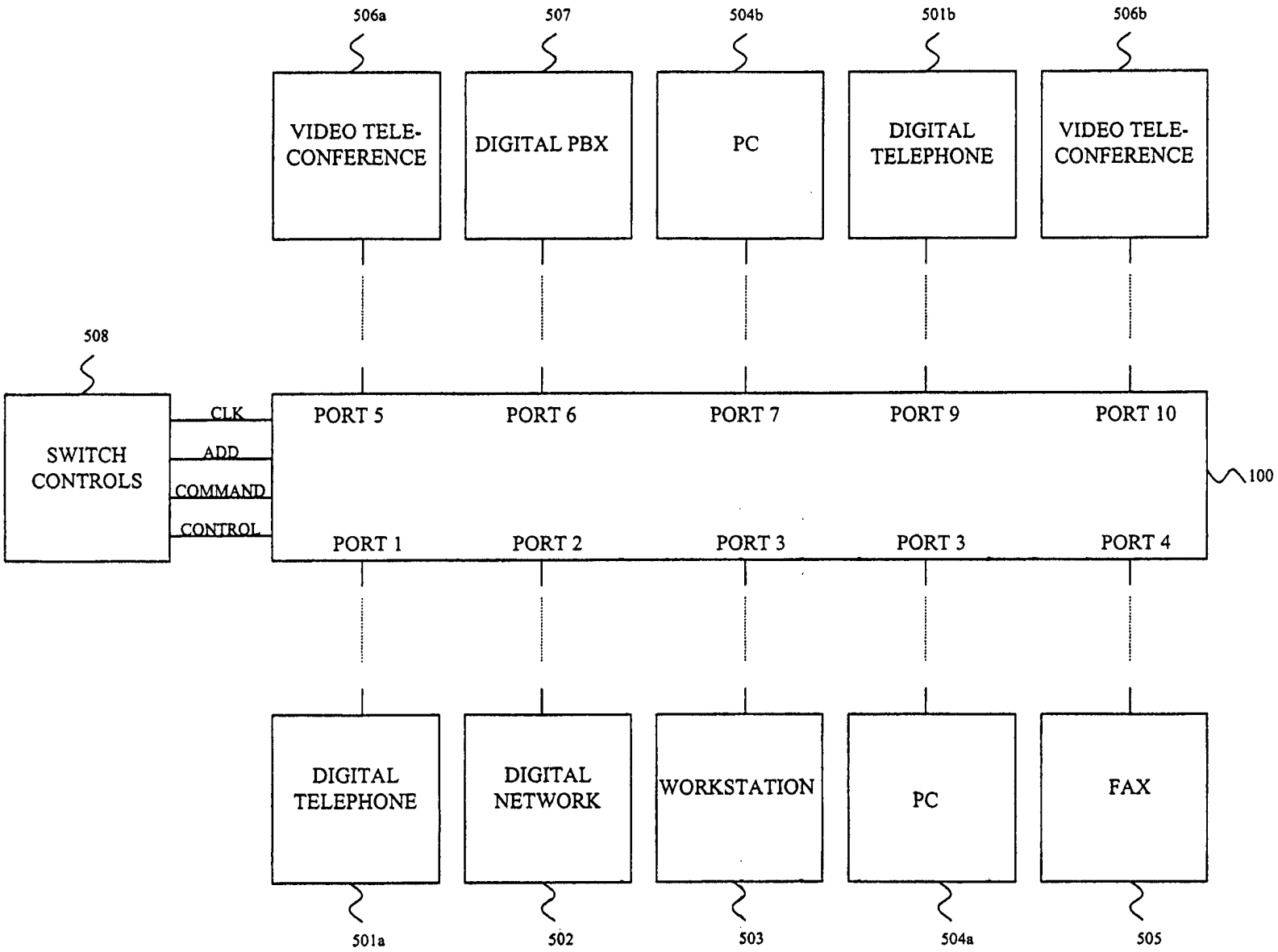

506a
507
504b
501b
506b
VIDEO TELE-CONFERENCE
DIGITAL PBX
PC
DIGITAL TELEPHONE
VIDEO TELE-CONFERENCE
508
SWITCH CONTROLS
CLK
ADD
COMMAND
CONTROL
PORT 5
PORT 6
PORT 7
PORT 9
PORT 10
100
PORT 1
PORT 2
PORT 3
PORT 3
PORT 4
DIGITAL TELEPHONE
DIGITAL NETWORK
WORKSTATION
PC
FAX
501a
502
503
504a
505

FIGURE 6

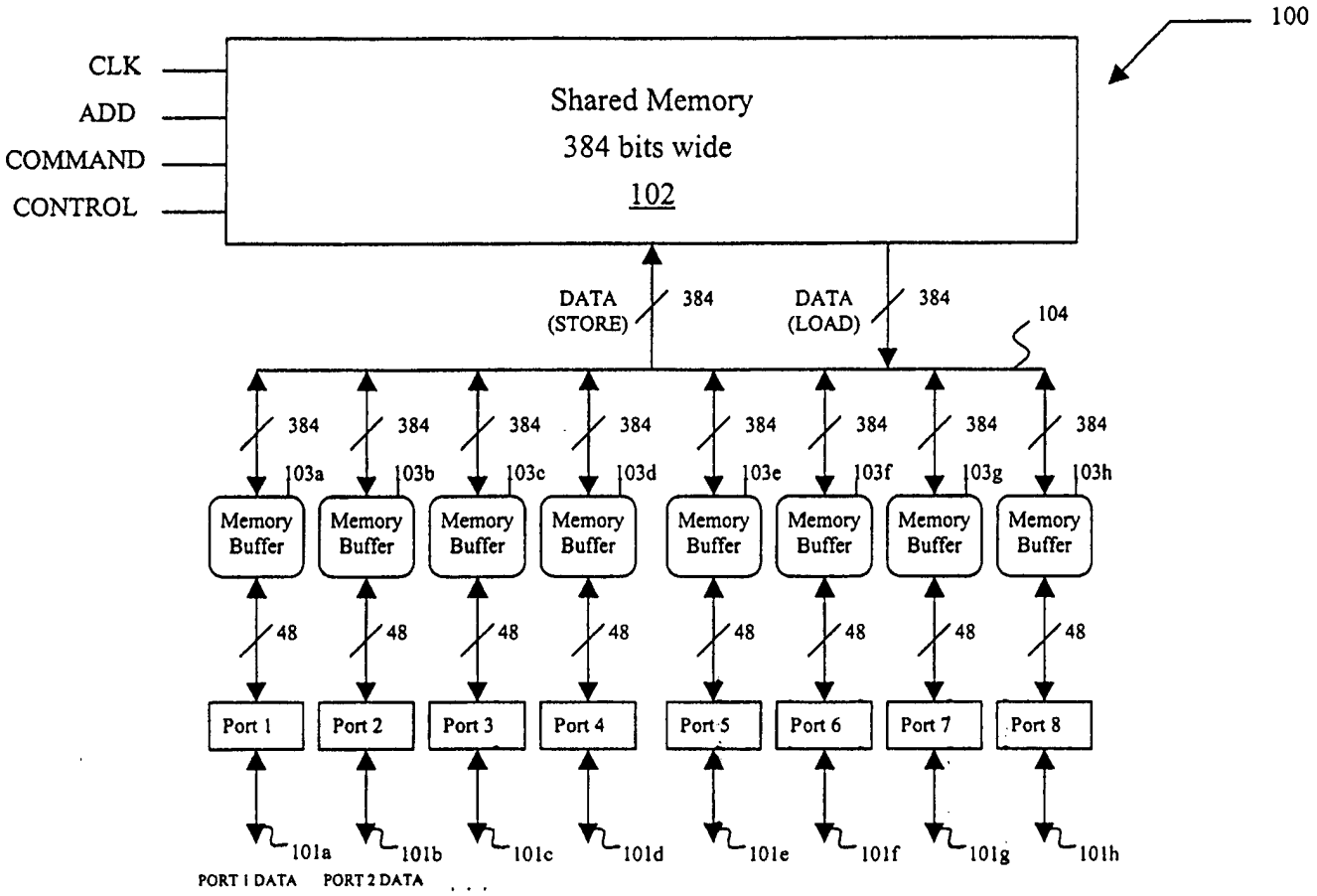

100
CLK
ADD
COMMAND
CONTROL
Shared Memory
384 bits wide
102
DATA (STORE)
384
DATA (LOAD)
384
104
384
103a
103b
103c
103d
103e
103f
103g
103h
Memory Buffer
48
Port 1
Port 2
Port 3
Port 4
Port 5
Port 6
Port 7
Port 8
101a
101b
101c
101d
101e
101f
101g
101h
PORT 1 DATA
PORT 2 DATA

FIGURE 7A

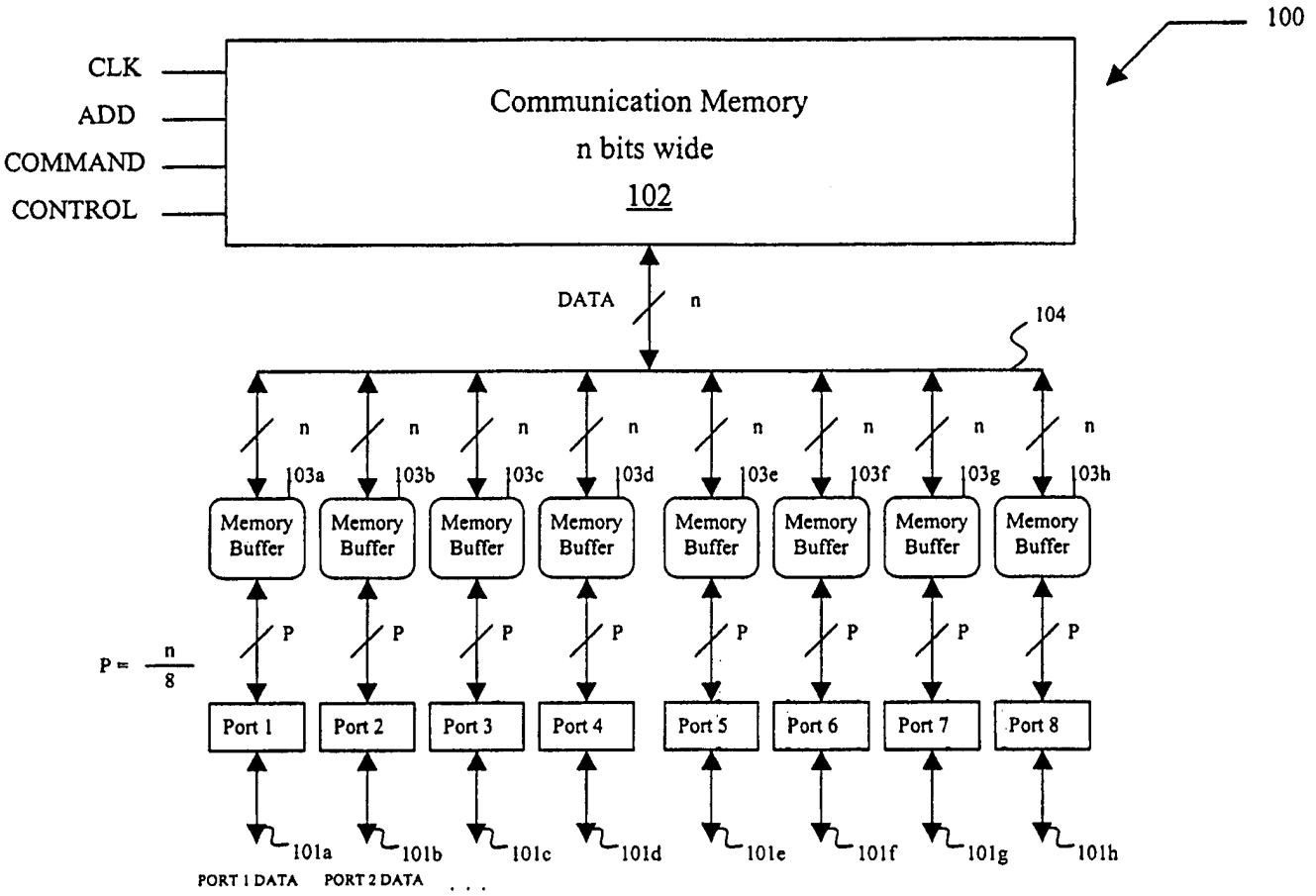

100
CLK
ADD
COMMAND
CONTROL
Communication Memory
n bits wide
102
DATA
n
104
n
103a
103b
103c
103d
103e
103f
103g
103h
Memory Buffer
P
P = n/8
Port 1
Port 2
Port 3
Port 4
Port 5
Port 6
Port 7
Port 8
101a
101b
101c
101d
101e
101f
101g
101h
PORT 1 DATA
PORT 2 DATA

FIGURE 7B

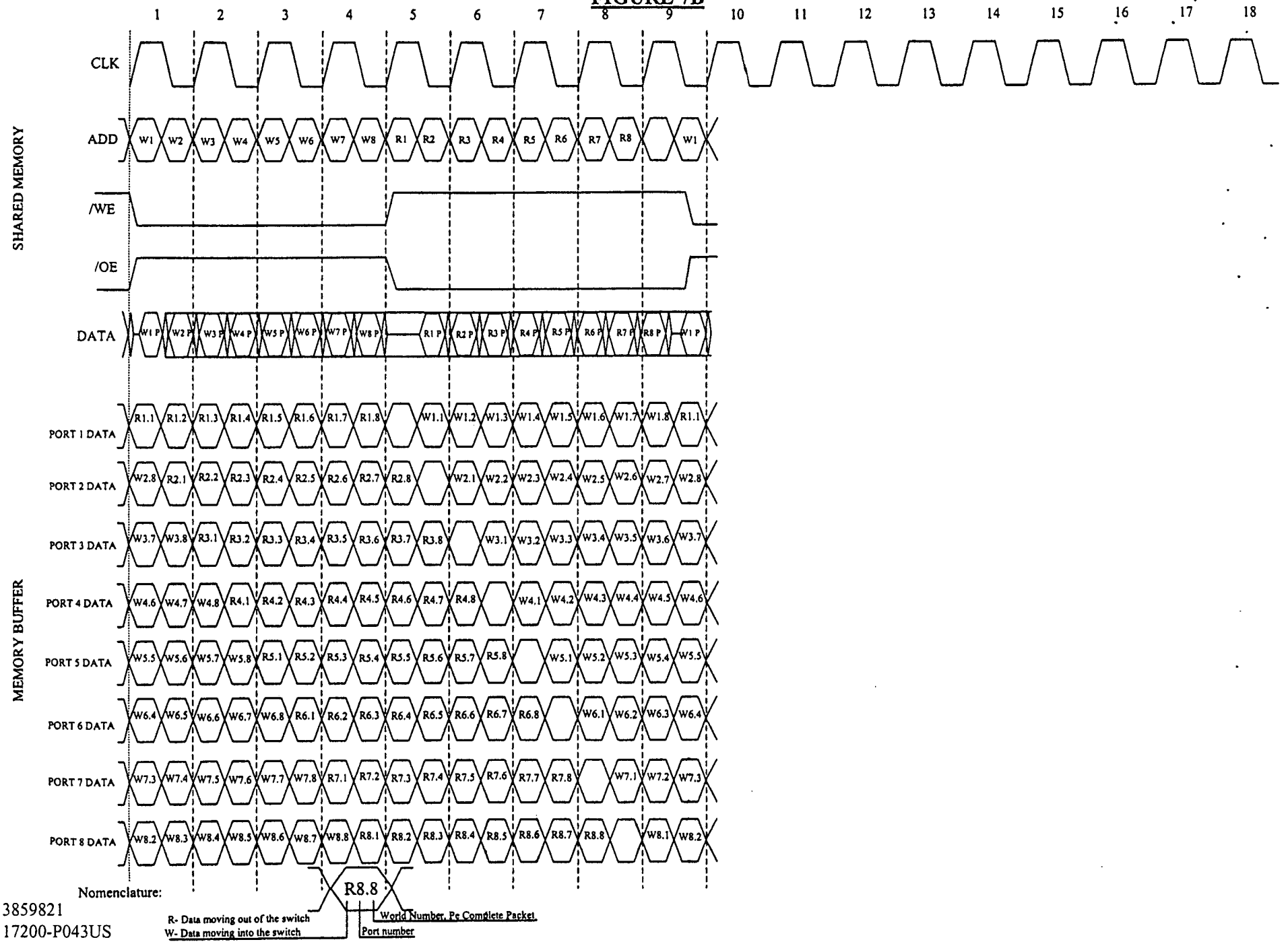


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FIGURE 8A

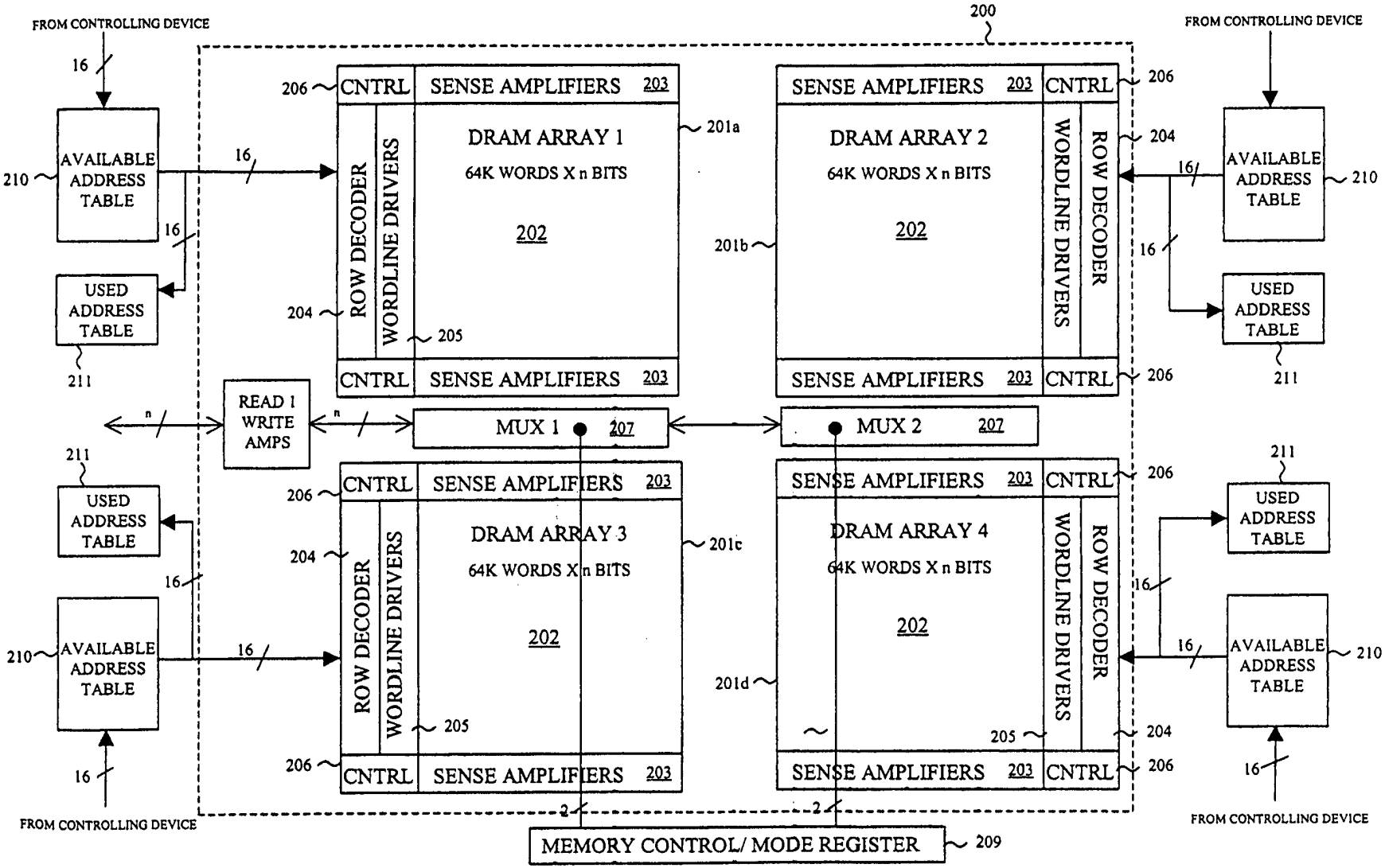

200
FROM CONTROLLING DEVICE
16
AVAILABLE ADDRESS TABLE
210
USED ADDRESS TABLE
211
206
CNTRL
SENSE AMPLIFIERS 203
ROW DECODER
WORDLINE DRIVERS
DRAM ARRAY 1
64K WORDS X n BITS
202
201a
204
205
201b
DRAM ARRAY 2
READ I WRITE AMPS
n
MUX 1 207
MUX 2 207
DRAM ARRAY 3
201c
DRAM ARRAY 4
201d
MEMORY CONTROL/ MODE REGISTER 209
2

FIGURE 8B

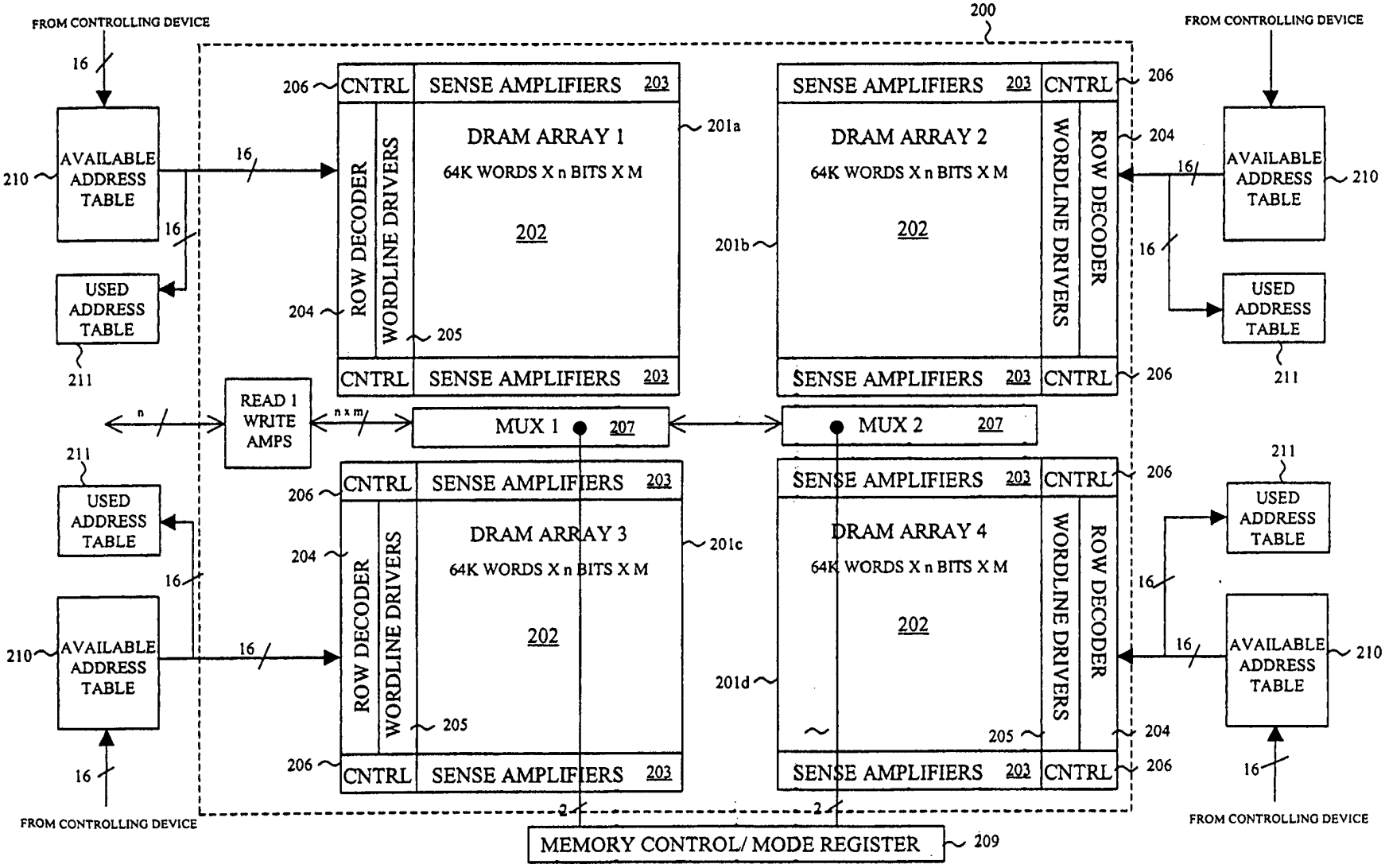

200
FROM CONTROLLING DEVICE
16
AVAILABLE ADDRESS TABLE
210
USED ADDRESS TABLE
211
206
CNTRL
SENSE AMPLIFIERS 203
ROW DECODER
WORDLINE DRIVERS
DRAM ARRAY 1
64K WORDS X n BITS X M
202
201a
204
205
DRAM ARRAY 2
201b
READ I WRITE AMPS
n
n x m
MUX 1 207
MUX 2 207
DRAM ARRAY 3
201c
DRAM ARRAY 4
201d
2
MEMORY CONTROL/ MODE REGISTER 209

FIGURE 8C

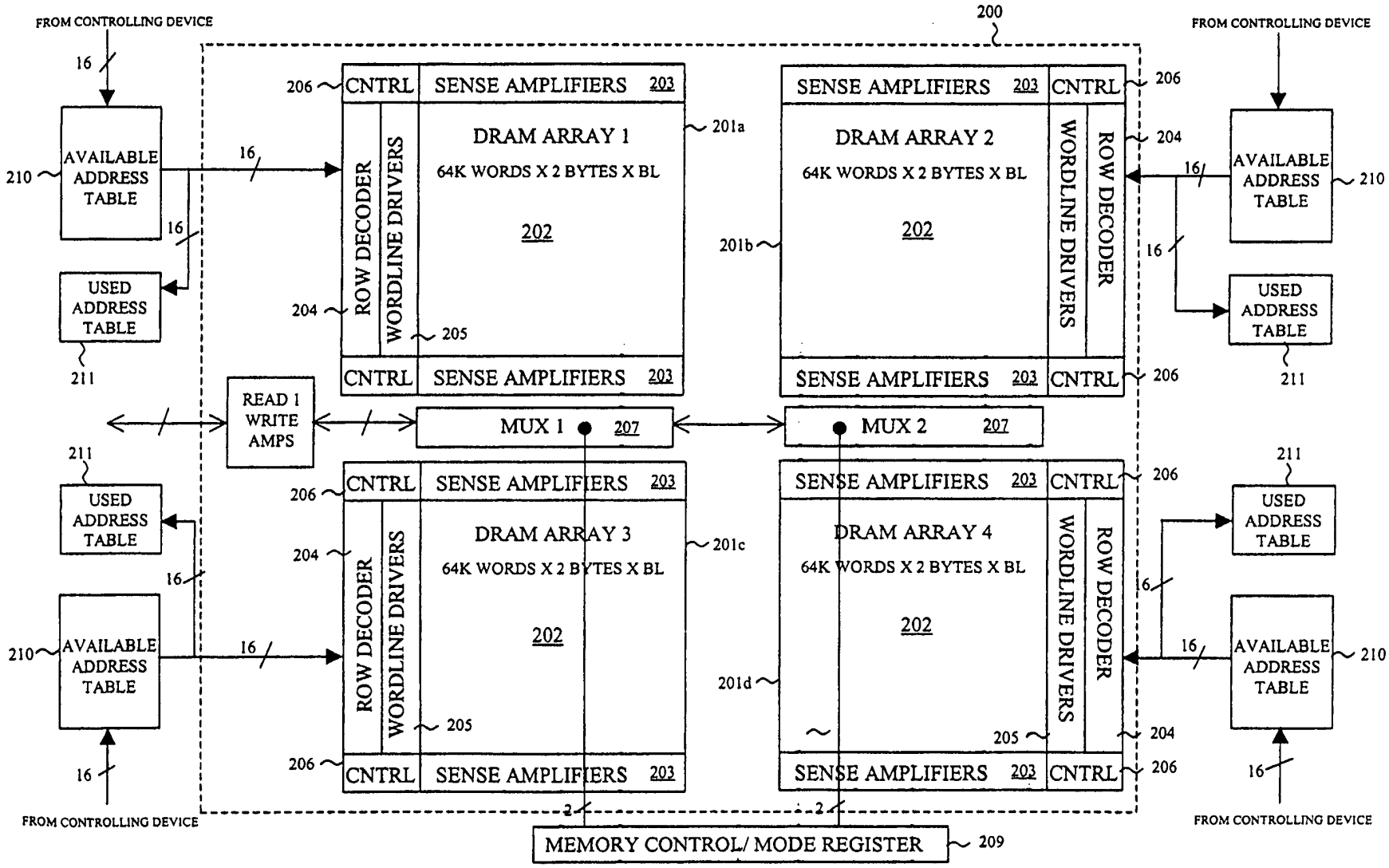

200
FROM CONTROLLING DEVICE
16
AVAILABLE ADDRESS TABLE
210
USED ADDRESS TABLE
211
206
CNTRL
SENSE AMPLIFIERS 203
ROW DECODER
WORDLINE DRIVERS
DRAM ARRAY 1
64K WORDS X 2 BYTES X BL
202
201a
204
205
DRAM ARRAY 2
201b
READ I WRITE AMPS
MUX 1 207
MUX 2 207
DRAM ARRAY 3
201c
DRAM ARRAY 4
201d
MEMORY CONTROL/ MODE REGISTER 209
2

FIGURE 9A

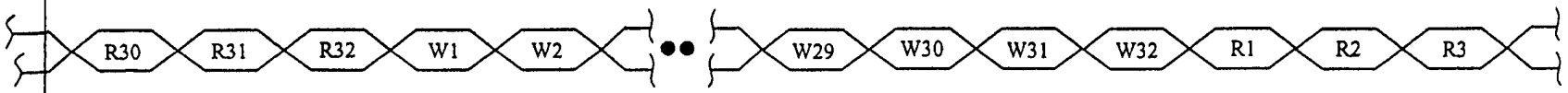


FIGURE 9B

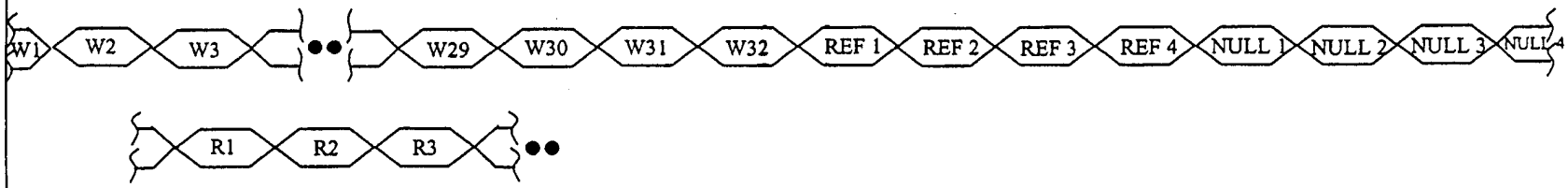


FIGURE 9C

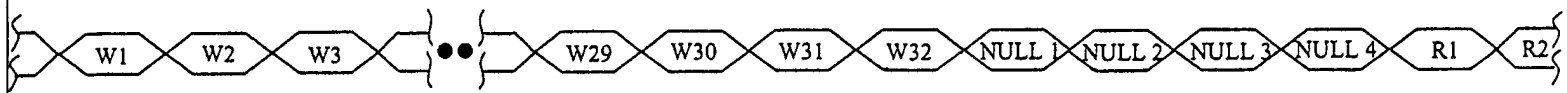


FIGURE 10

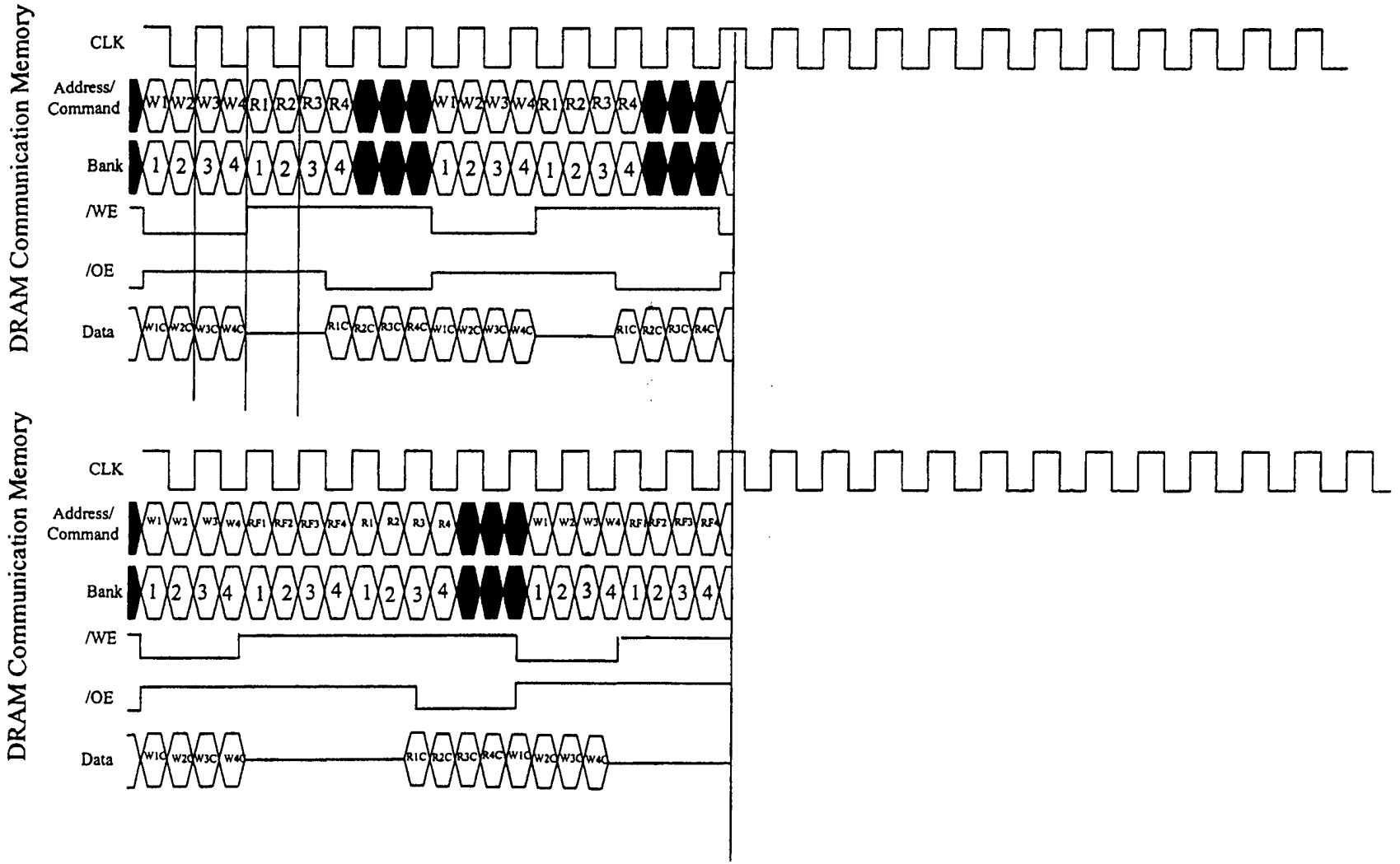
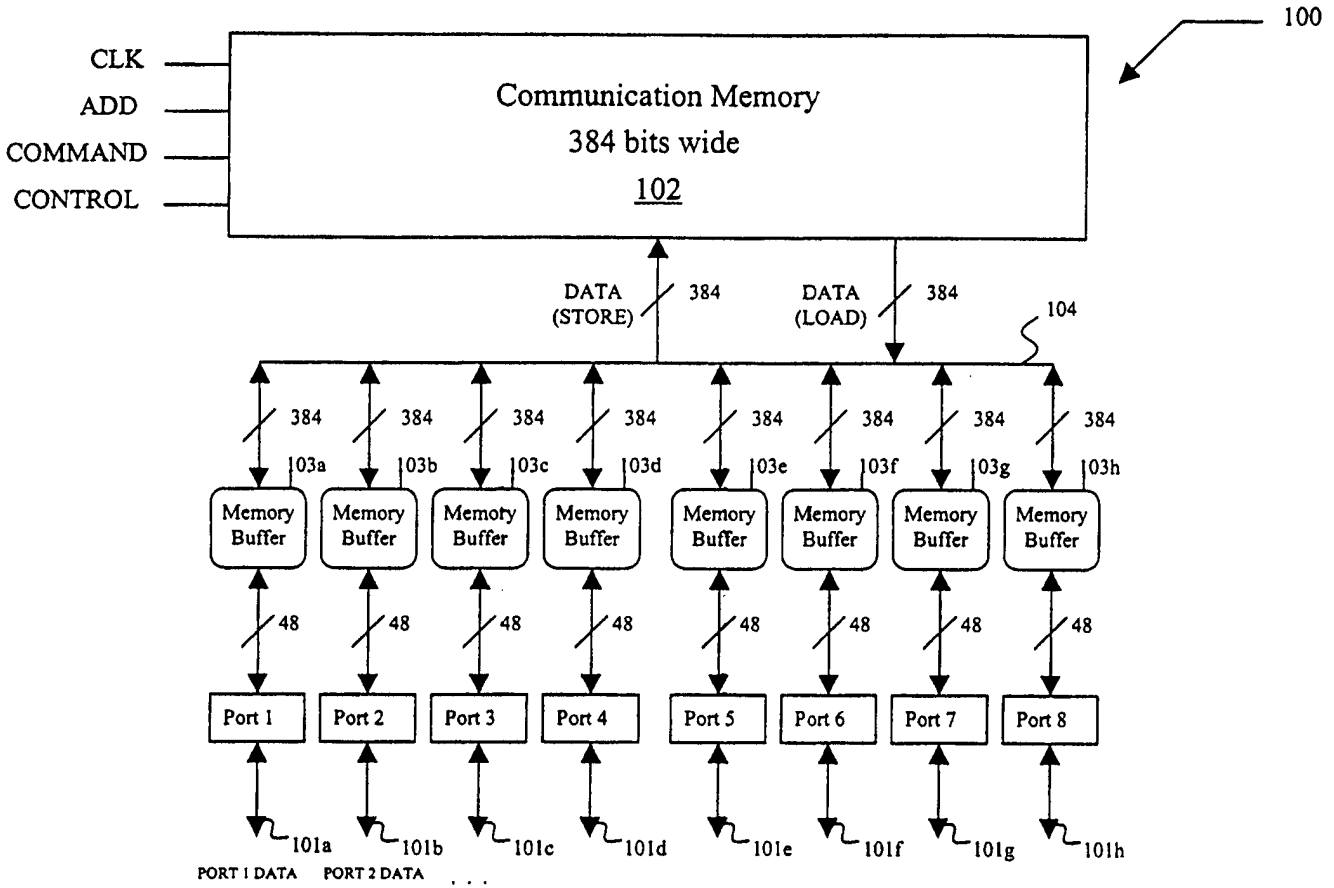

DRAM Communication Memory
CLK
Address/ Command
Bank
/WE
/OE
Data
DRAM Communication Memory
CLK
Address/ Command
Bank
/WE
/OE
Data

FIGURE 11


100
CLK
ADD
COMMAND
CONTROL
Communication Memory
384 bits wide
102
DATA (STORE)
384
DATA (LOAD)
384
104
384
03a
03b
03c
03d
03e
03f
03g
03h
Memory Buffer
48
Port 1
Port 2
Port 3
Port 4
Port 5
Port 6
Port 7
Port 8
101a
101b
101c
101d
101e
101f
101g
101h
PORT 1 DATA
PORT 2 DATA